AMENDMENTS TO THE SPECIFICATION

Replace the paragraph starting at page 1, line 18, with the following replacement paragraph:

A particular concern in implementing an IEEE ~~802.11~~ 802.11a based OFDM PHY in hardware involves providing a cost-effective, compact device the can be implemented in smaller wireless devices. Hence, implementation concerns typically involve cost, device size, and device complexity.

Replace the paragraph starting at page 3, line 15, with the following replacement paragraph:

Figure 1 is a diagram illustrating a conventional (PRIOR ART) direct conversion receiver configured for recovering I and Q components from a received IEEE ~~802.11~~ 802.11a OFDM wireless signal.

Replace the paragraph starting at page 3, line 17, with the following replacement paragraph:

Figure 2 is a diagram illustrating the receiver portion of an IEEE ~~802.11~~ 802.11a OFDM transceiver according to an embodiment of the present invention.

Replace the paragraph starting at page 3, line 29, with the following replacement paragraph:

The disclosed embodiment will be described with reference to an overview of an IEEE ~~802.11~~ 802.11a OFDM transceiver, followed by a detailed description of the I/Q compensation module implemented according to an embodiment of the present invention.

Replace the paragraph starting at page 4, line 4, with the following replacement paragraph:

Figure 2 is a diagram illustrating an architecture of a receiver module 50 of an IEEE ~~802.11~~ 802.11a Orthogonal Frequency Division Multiplexing (OFDM) transceiver, according to an embodiment of the present invention. The receiver module 50, implemented as a digital circuit, includes an I/Q mismatch compensation module 52 that receives detected wireless signal samples (in digital form) from an R/F analog front end (AFE) amplifier 40 having an analog to digital (A/D) converter. The gain of the AFE amplifier 40 is controlled by an AGC module 55. The detected wireless signal samples include an I component and Q component: these I and Q components, which ideally should be orthogonal to each other and have a uniform relative gain, may in fact have a non-orthogonal phase difference (i.e., other than 90 degrees) and have an unequal gain. Hence, the I/Q mismatch compensation module 52 is configured for compensating the mismatched I/Q components to generate compensated signal samples having matched I/Q components with orthogonal phase difference and a uniform relative gain.

Replace the paragraph starting at page 5, line 18, with the following replacement paragraph:

Since certain tones output by the FFT 64 may have encountered fading due to signal attenuation and distortion on the wireless channel, equalization is necessary to correct the fading. The frequency domain equalizer 68 is configured for reversing the fading encountered by the tones in order to provide equalized tones. Channel information is obtained by the channel estimator 70 from the long training sequence in the IEEE ~~802.11~~ 802.11a preamble; the channel information is used by the channel estimator 70 to estimate the channel characteristics; the estimated channel characteristics are supplied to the frequency equalizer 68 to enable equalization of each tone.

Replace the paragraph starting at page 5, line 30, with the following replacement paragraph:

The decoding portion 80 includes a digital slicer module 82, a deinterleaver 84, and a Viterbi decoder 86. The digital slicer module recovers up to 6 bits of symbol data from each tone, based on the data rate specified in the signal field in the preamble. The deinterleaver 84 performs the converse operation of the transmitter interleaver circuit, and rearranges the data back into the proper sequence of deinterleaved data. The Viterbi decoder 86 is configured for decoding the deinterleaved data into decoded data, in accordance with the IEEE ~~802.11~~ 802.11a specification.

Replace the paragraph starting at page 6, line 3, with the following replacement paragraph:

The descrambler circuit 90 is configured for recovering the original serial bit stream from the decoded data, by descrambling a 127-bit sequence generated by the scrambler of the transmitter, according to the IEEE ~~802.11~~ 802.11a specification. The descrambler circuit 90 utilizes a scrambling seed, recovered from the service field of the data packet by the seed estimation circuit 92, for the descrambling operation. The signal field information from the preamble also is stored in a signal field buffer 94, configured for storing the length and data rate of the payload in the data packet. Overall control of the components of the receiver 50 is maintained by the state machine 96.

Replace the paragraph starting at page 6, line 10, with the following replacement paragraph:

Hence, the serial bit stream recovered by the descrambler circuit 90 is output to an IEEE ~~802.11~~ 802.11a compliant Media Access Controller (MAC).